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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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FACSIMILE COVER SHEET

X	FACSIMILE COVER SHEET	___	AMENDMENT (# Pages)
___	NEW APPLICATION	X	EOT (2 Month)
___	DECLARATION (# Pages)	___	NOTICE OF APPEAL
___	ASSIGNMENT (# Pages)	X	APPEAL (7 Pages)
___	FORMAL DRAWINGS	___	ISSUE FEE (# Pages)
___	INFORMAL DRAWINGS	___	CHANGE IN CORRESPONENCE ADDRESS
___	CONTINUATION APP'N (# Pages)		
___	DIVISIONAL APP'N		

NAME OF INVENTOR(S): Torres

RECEIPT DATE & SERIAL NO.:

Serial No.: 10/614,846

Filing Date: 7/8/2003

TITLE OF INVENTION: HIGH SPEED, LOWER POWER LVDS DRIVER

TI FILE NO.: TI-35321

DEPOSIT ACCT. NO.: 20-0668

FAXED: 6-2-05
DUE: 04/04/2005
ATTY/SECY: WDS/slh

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Torres	Docket No:	TI-35321
Serial No:	10/614,846	Examiner:	Wells, Kenneth
Filed:	7/8/2003	Art Unit:	2816
For:	HIGH SPEED, LOWER POWER LVDS DRIVER		

APPEAL BRIEF PURSUANT TO 1.192(c)

CERTIFICATION OF FACSIMILE TRANSMISSION

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Sharlet Hurst

Sharlet Hurst

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

The following Appeal Brief is respectfully submitted in connection with the above identified application in response to the Final Office Action mailed November 15, 2004, and the Advisory Action mailed January 28, 2005.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated.

RELATED APPEALS AND INTERFERENCES

Appellants legal representative knows of no appeals or interferences which will be directly affected, or have a bearing on the Board's decision.

STATUS OF THE CLAIMS

Claims 1-26 were originally filed, with Claims 16-26 standing cancelled. Consequently, the subject matter of the instant appeal is the rejection of Claims 1-15.

STATUS OF AMENDMENTS

A Response After Final was filed on January 21, 2005, amending Claim 1.

The Advisory Action indicated that the proposed amendment would be entered.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Referring now to Figure 2, a driver circuit 20 of the present invention is presented. The driver circuit 20 comprises a differential pair 22 comprising a first pair of transistors Q1 and Q2, coupled to a pair of inputs A and B via a first pair of tri-state switches MN1 and MN2 (which may also be very small transistors), that are coupled to one another and to a logic pin ZST that is always high, thus forming a closed switch for the propagation of data from the input A to transistor Q1, and from the input B to the transistor Q2. The first pair of transistors Q1 and Q2 are respectively coupled to a first pair of parallel coupled resistors R1 and R2 via a first pair of nodes N1 and N2. The first pair of parallel coupled resistors R1 and R2 are coupled to a voltage regulator 24.

The first pair of nodes N1 and N2 are respectively coupled to a second pair of transistors Q3 and Q4 which are further coupled to one another and to a node ISREF which can limit an amount of current that the transistors Q3 and Q4 can pass. The second pair of transistors Q3 and Q4, which form a voltage drive stage 26, are further respectively coupled to a load resistance RL via second pair of nodes N3 and N4. The second pair of nodes N3 and N4 are further respectively coupled to a resistor RF1 and an output node Y, and to a resistor RF2 and an output node Z.

The second pair of nodes N3 and N4 are also respectively coupled to a second pair of tri-state switches MN3 and MN4 which are further respectively coupled to the input nodes B and A.

The serially coupled transistor Q5 and the resistor R5, as well as the serially coupled transistor Q6 and the resistor R6, and the serially coupled transistor Q7 and the resistor R7 form the biasing circuitry 30. The transistor Q5 is coupled to the transistor Q6 which is coupled to the transistor Q7 and to the first pair of transistors Q1 and Q2. The resistors R5-R7 are coupled to a ground node.

GROUNDS OF REJECTION

The two issues on appeal are first whether Claims 1, 2, and 13-15 are anticipated under 35 U.S.C. § 102 by Urakawa; and second whether Claims 3-12 are unpatentable under 35 U.S.C. § 103 over Urakawa.

ARGUMENTS

It is respectfully submitted that Urakawa does not disclose or suggest the presently claimed invention including the differential first pair of transistors to input a differential signal and a current switch coupled to the second pair of nodes to steer the current based on the polarity of the first pair of input nodes.

Urakawa discloses a single input A to transistor Q1. No differential signal or consequently the differential first pair of transistors is seen.

The Examiner alleges that the differential signal that the input signal is not part of the claimed invention and the circuit of Urakawa is capable of receiving a differential signal.

Applicants traverse these allegations of the Examiner.

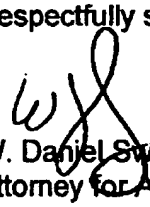
First, the differential signal is part of the claimed invention and further there is no evidence that Urakawa discloses a differential signal and consequently what the circuit is capable of is speculative.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1-15 under 35 U.S.C. § 102 and 35 U.S.C. § 103 is not properly founded in law, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejections.

To the extent necessary, the Appellants petition for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,



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APPENDIX

Claim 1 (previously presented): A driver circuit, comprising:

a differential first pair of transistors to input a differential signal;

a voltage drive stage comprising a second pair of transistors;

a first pair of nodes coupled to the first pair of transistors and to the second pair of transistors;

a second pair of nodes coupled to the second pair of transistors; and

a current switch coupled to the second pair of nodes to steer current based the polarity of said first pair of nodes.

Claim 2 (original): The driver circuit of claim 1 further comprising a first pair of resistors coupled to the first pair of nodes.

Claim 3 (original): The driver circuit of claim 2 further comprising a voltage regulator coupled to the first pair of resistors.

Claim 4 (original): The driver circuit of claim 1 further comprising a load resistor coupled to the second pair of nodes.

Claim 5 (original): The driver circuit of claim 1 further comprising a second pair of resistors coupled to the second pair of nodes.

Claim 6 (original): The driver circuit of claim 5 further comprising a pair of output nodes coupled to the second pair of resistors.

Claim 7 (original): The driver circuit of claim 5 further comprising an output voltage coupled to the second pair of resistors.

Claim 8 (original): The driver circuit of claim 1 further comprising three serially coupled transistor and resistor pairs, wherein the first serially coupled

transistor is coupled to an input node, wherein the second serially coupled transistor is coupled to the differential first pair of transistors, and wherein the third serially coupled transistor comprises a portion of the dynamic current switch.

Claim 9 (original): The driver circuit of claim 8, wherein the first transistor is coupled to the second transistor.

Claim 10 (original): The driver circuit of claim 8, wherein the second transistor is coupled to the third transistor.

Claim 11 (previously presented): The driver circuit of claim 8, further comprising a ground, wherein the three resistors of the serially coupled transistor and resistor pairs are coupled to the ground.

Claim 12 (previously presented): The driver circuit of claim 8, further comprising an additional transistor coupled to the input node.

Claim 13 (original): The driver circuit of claim 1, wherein a first one of the first pair of nodes follows a first one of the second pair of nodes.

Claim 14 (original): The driver circuit of claim 1, wherein a second one of the first pair of nodes follows a second one of the second pair of nodes.

Claim 15 (original): The driver circuit of claim 1, further comprising a pair of input nodes coupled to the differential first pair of transistors and to the dynamic current switch.

Claims 16-26 (cancelled)

EVIDENCE APPENDIX

Appellants are submitting no items of evidence.

RELATED PROCEEDINGS APPENDIX

Appellants have no submission for the Related Proceeding Appendix.